REMARKS

At the time of the Office Action dated April 23, 2004, claims 9-25 were pending and rejected in this application. Claims 9, 11, 13, 19-20, 24-25 have been amended, and claims 12, 18 and 23 have been cancelled. Care has been exercised to avoid the introduction of new matter. Claim 9 has been amended by incorporating the limitations of claim 12 therein, and consequently claim 12 has been cancelled. Claim 11 has been amended to address an informality issue. Claim 13 has been amended by incorporating the limitations of claim 18 therein, and consequently claim 18 has been cancelled. Claim 19 has been amended to address a dependency issue arising from the cancellation of claims 18. Claim 20 has been amended by incorporating the limitations of claim 23 therein, and consequently claim 23 has been cancelled. Claims 24 and 25 have been amended to address dependency issues arising from the cancellation of claims 23. Applicants have also amended the specification to add the reference numerals 41, 41a, 41b, shown in Figs. 17 and 21. Applicant submits that the present Amendment does not generate any new matter issue.

On page two of the Office Action, the Examiner objected to claims 11 and 12, asserting that there is insufficient antecedent basis for the term "said sense amplifiers" since only one sense amplifier had been previously recited. In response, Applicant notes that claim 11 has been amended to delete the term "said sense amplifiers" and in its place insert the term "said sense amplifier." Applicant, therefore, respectfully solicits withdrawal of the imposed objection of claims 11 and 12.

CLAIMS 13-19 ARE REJECTED UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY TOBITA, U.S. PATENT NO. 6,388,934

On page three of the Office Action, the Examiner asserted that Tobita discloses a semiconductor memory device corresponding to that claimed. This rejection is respectfully traversed.

The Examiner alleges that Fig. 1 of Tobita teaches each element of the claimed invention including a memory cell array (MC1 – MCn) and a sense amplifier (SA and RSA) connected to the bit lines and used for amplifying a signal for access to said memory cells and refresh, wherein memory cells (e.g., MC1) are paired with complementary memory cells (e.g., MC2). Tobita is also alleged to teach the sense amplifier is formed of a normal sense amplifier (SA) connected to the bit line coupled to the memory cell and a complementary sense amplifier (RSA) connected to a complementary bit line coupled to the complementary memory cell. Tobita is also alleged to teach that the word lines are formed of a first word line (WL1) and a second word line (WL2) and that one of the transistors in the memory cell is arranged as a transistor for normal access (NQ) and the other is arranged for refresh (RQ).

In response, Applicant notes that independent claim 13 has been amended to include the limitations previously presented in claim 18. Specifically, claim 13 now recites switching control means. The factual determination of anticipation under 35 U.S.C. § 102 requires the identical disclosure of each element of a claimed invention in a single reference. As part of this analysis, the Examiner must (a) identify the elements of the claims, (b) determine the meaning of

the elements in light of the specification and prosecution history, and (c) identify corresponding elements disclosed in the allegedly anticipating reference. That burden has not been discharged.

Although the Examiner asserts that the limitations previously presented in claim 18 are identically disclosed by Tobita, the Examiner fails to indicate where Tobita teaches the claimed switching means. In fact, the statement of the rejection is completely silent as to the claimed switching means. In this regard, the Examiner's rejection under 35 U.S.C. § 102 also fails to comply with 37 C.F.R. § 1.104(c),[1] which requires that the Examiner clearly designate the teachings in the applied reference being relied upon. Applicant has also reviewed Tobita and is unable to identify a feature taught by Tobita that corresponds to the claimed switching means. Therefore, Tobita fails to identically describe the claimed invention, as recited in amended claim 13, within the meaning of 35 U.S.C. § 102. Applicant, thus, respectfully solicits withdrawal of the imposed rejection of claims 13-17 and 19 under 35 U.S.C. § 102 for anticipation based upon Tobita.

CLAIMS 9-12 ARE REJECTED UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY WANLASS, U.S. PATENT NO. 4,203,159

On page four of the Office Action, the Examiner asserted that Wanlass discloses a semiconductor memory device corresponding to that claimed. Specifically, Wanlass is alleged to teach a semiconductor memory device comprising a memory cell array (Fig. 1), a sense amplifier

[1] 37 C.F.R. § 1.104(c) provides:

> In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

(27, 54; Fig. 1), wherein a first transistor arranged as a transistor for normal access to be used for the normal access and not to be used for the refresh access (12, col. 2, lines 51-56), and a second transistor arranged as a transistor for refresh to be used for the refresh access and not to be used for the normal access (13, col. 5, lines 33-41). This rejection is respectfully traversed.

Independent claim 9 has been amended to include the limitations previously presented in claim 12. Specifically, claim 9 now recites that the semiconductor memory device employs a background refresh system for automatically refreshing a memory cell regardless of presence and absence of a refresh signal when an access sense amplifier is operating. Upon reviewing the statement of the rejection regarding claims 9-12, Applicant notes that the statement of the rejection does not identify any feature in Wanlass that corresponds to the claimed background refresh system. Furthermore, Applicant has also reviewed Wanlass and is unable to identify a feature taught by Wanlass that corresponds to the claimed background refresh system. Since the Examiner has not identified where Wanlass teaches the claimed background refresh system, Applicant submits that a prima facie case of anticipation has not been made by the Examiner. Furthermore, since the claimed background refresh system is not disclosed by Wanlass, Applicant respectfully solicits withdrawal of the imposed rejection of claims 9-11 under 35 U.S.C. § 102 for anticipation based upon Wanlass.

CLAIMS 20-25 ARE REJECTED UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY CASPER, U.S. PATENT NO. 5,822,258

On pages four and five of the Office Action, the Examiner asserted that Casper discloses a semiconductor memory device corresponding to that claimed. Specifically, Wanlass is alleged

to teach in Fig. 1 a memory device 100 comprising a memory array 102 of cells 104, a cell plate 110 forming an electrode of a capacitor 108 and using the impurity region (col. 3, lines 40-42) as an opposite electrode and cell plate potential changing means 112 for changing the potential on the cell plate. The Examiner also alleges that Casper teaches that the cell plate is a "time-varying potential changing means for correcting the potential on said cell plate varying with time due to leak of potentials in said capacitor" (citing col. 4, lines 18-19). This rejection is respectfully traversed.

Independent claim 20 has been amended to include the limitations previously presented in claim 23. Specifically, claim 20 now recites that the cell plate potential changing means is a time-varying potential changing means for correcting the potential on a cell plate varying with time due to leak of potentials in a capacitor. In the statement of the rejection, the Examiner identified feature 112 as the claimed cell plate potential changing means. Applicant respectfully disagrees.

Casper notes the problem of defective cells created during memory cell fabrication and discloses a voltage generator 112, which aids in the detection of defective cells by providing one of two different drive currents (i.e., a normal current and a test current)(col. 4, lines 4-8). Prior to normal operation, the memory devices 100 are tested to identify cells with defective capacitors (col. 3, lines 64-66). If, during such test, a variance in the voltage on cell plate 110 is detected, the memory cell is deemed defective, whereupon it is presumably repaired out with extra memory cells (col. 1, lines 55-57). Therefore, Casper does not identically teach a "time-varying potential changing means for correcting the potential on said cell plate varying with time due to

leak of potentials in said capacitor," as described in the fourth embodiment of the invention and recited in amended claim 20. Applicant, therefore, respectfully solicits withdrawal of the imposed rejection of claims 20-22 and 24-25 under 35 U.S.C. § 102 for anticipation based upon Casper.

Applicant has made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicant invites the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing remarks, Applicant hereby respectfully requests reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

Respectfully submitted,

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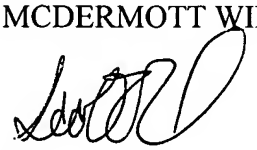

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